Name:

Maaz Habib

Lab Course Title:

Digital Logic Design

Semester:

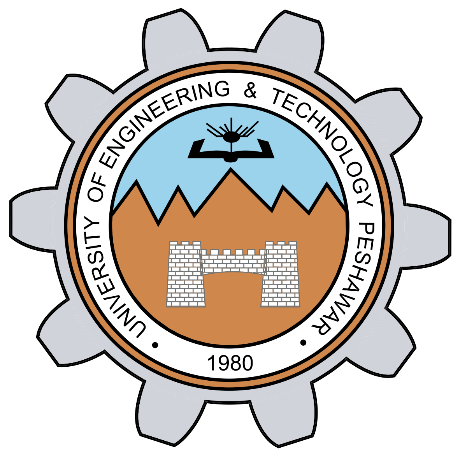
3rd Semester

Registration No.

20pwcse1952

**DLD Lab**

**Department of Computer System Engineering**

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Submitted to:

Engr. Faiz Ullah

**University of Engineering & Technology, Peshawar Department of Computer System Engineering**

**DLD Lab # 10**

**J-K and T Flip Flop**

**Aim:**

Verification of state tables of J-K flip-flop and T flip-flop using AND gate and NOR gates.

**Apparatus:**

IC 7402 (NOR Gate), IC 7411 (AND Gate).

**What is Flip-Flop:**

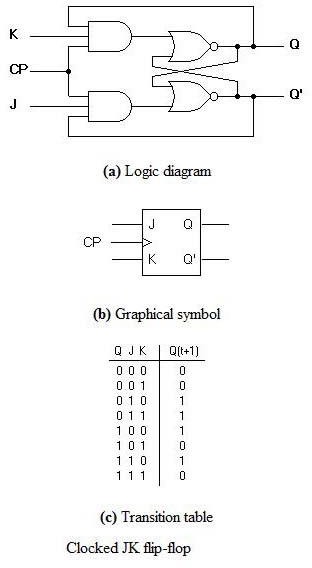
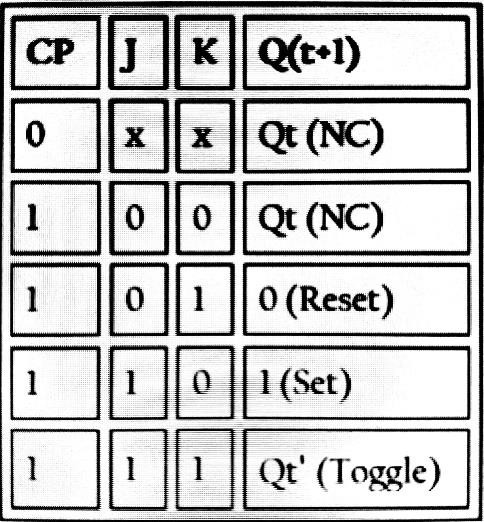
The basic 1-bit digital memory circuit is known as flip-flop. It can store either 0 or 1. Flip-flops are classifieds according to the number of inputs.

**Latch vs Flip-Flop:**

The circuit is similar to latch except enable signal is replaced by clock pulse.

**J-K Flip Flop:**

The J-K flip-flop is the most versatile of the basic flip-flops. It has the input following character of the clocked D flip-flop but has two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge.

The circuit diagram and truth-table of a J-K flip flop is shown below.

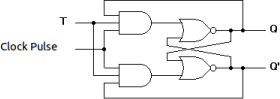
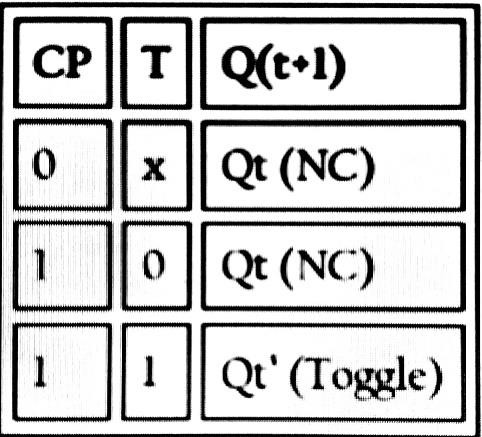
**Truth table of J-K flip-flop**

**Other definition of J-K:**

A J-K flip flop can also be defined as a modification of the S-R flip flop. The only difference is that the intermediate state is more refined and precise than that of a S-R flip flop. The behavior of inputs J and K is same as the S and R inputs of the S-R flip flop. The letter J stands for SET and the letter K stands for CLEAR.

The circuit includes two 3-input AND gates. The output Q of the flip flop is returned back as feedback to the input of the AND along with other inputs like K and clock pulse [CP]. So, if the value of CP is ‘1’, the flip flop gets a CLEAR signal and with the condition that the value of Q was earlier 1. Similarly output Q’ of the flip flop is given as feedback to the input of the AND along with other inputs like J and clock pulse [CP]. So, the output becomes SET when the value of CP is 1 only if the value of Q’ was earlier 1. The output may be repeated in transitions once they have been complimented for J=K=1 because of the feedback connection in the JK flip-flop. This can be avoided by setting a time duration lesser than the propagation delay through the flip-flop. The restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction.

**T Flip Flop:**

 T flip – flop is an edge triggered device i.e., the low to high or high to low transitions on the input clock signal will cause a change in the output state of the flip – flop. This is a much simpler version of the J-K flip flop. Both the J and K inputs are connected together and thus are also called a single input J-K flip flop. When clock pulse is given to the flip flop, the output begins to toggle. Here also the restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction. Take a look at the circuit and truth table below.

Truth table of T-Flip-Flop

**Procedure:**

1. Connections are made as per circuit diagram.

2. Verify truth- tables for various combinations of input.

**Precaution:**

1. All the ICs should be checked before using the apparatus.
2. All LEDs should be checked.
3. All connections should be tight.
4. Always connect GROUND first and then VCC.
5. The circuit should be off before changing the connections.
6. After completing the experiment switch off the supply to apparatus.

**Lab Questions:**

1. **Differentiate between combinational and sequential circuits.**

Ans. A circuit whose output is dependent only on the inputs at that instant is called combinational circuit. And a circuit whose output is dependent on present and past history of the inputs is called sequential circuit.

1. **What is a latch?**

Ans. Storage elements that operate with signal levels are referred to as latches.

1. **What is a flip-flop?**

Ans. Storage elements controlled by clock transitions are called flip-flops.